

Applic. No.: 10/631,356  
Amdt. Dated February 2, 2006  
Reply to Office action of November 2, 2005

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Amendments to the Specification:

Please replace the paragraph on page 14, lines 1-3, with the following paragraph:

Fig. 4 is a table showing four command sequences used in testing the semiconductor memory from Fig. 3 according to the invention; and

Please replace the paragraph on page 14, line 5, with the following paragraph:

Fig. 5 is an excerpt from a command sequence from Fig. 4[[.]]<sub>i</sub>  
and

Please insert the following paragraph after page 14, line 5:

Fig. 6 is a flow chart showing the steps of the testing method according to the invention.

Please replace the abstract of the disclosure with the following:

A testing method ~~for testing a semiconductor memory having a plurality of memory banks~~ involves information being written to memory addresses ~~and/or~~ and being read from the memory

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addresses. The method which logically combines parallel memory bank actuation of the memory addresses using an interleaved mode, which is implemented in relation to disjunct subareas of the memory banks, with one another. This shortens the test time required for testing the semiconductor memory.